BTeV Trigger (WBS 1.8) and Data Acquisition System (WBS 1.9)

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Overview

- Introduction
- Trigger & data acquisition system (DAQ) architecture
- WBS 1.8 – Trigger electronics & software
  - Project management overview
  - Major components of the trigger
  - Trigger R&D (used for cost and schedule estimates)
  - Cost, schedule, milestones, and risk analysis
- WBS 1.9 – DAQ electronics & software
  - Project management overview
  - Major components of the DAQ
  - Cost, schedule, milestones, and risk analysis
- Presentations prepared for the breakout sessions

Introduction

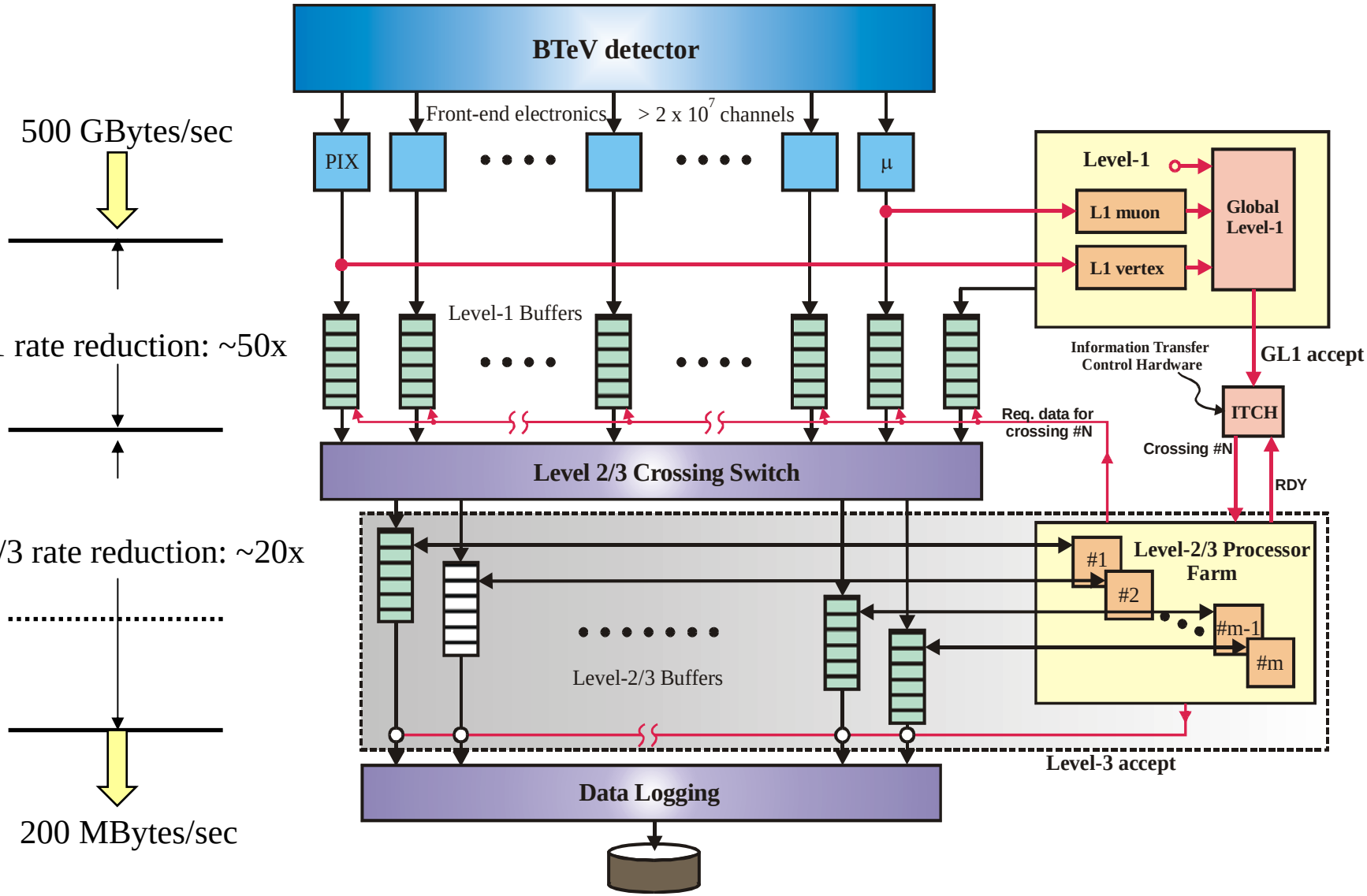
- The challenge for the BTeV trigger and data acquisition system is to reconstruct particle tracks and interaction vertices for **EVERY** interaction that occurs in the BTeV detector, and to select interactions with *B* decays.
- The trigger performs this task using 3 stages, referred to as Levels 1, 2, and 3:
  "L1" – looks at every interaction, and rejects at least 98% of min. bias background
  "L2" – uses L1 computed results & performs more refined analyses for data selection
  "L3" – performs a complete analysis using all of the data for an interaction

Reject > 99.9% of background. Keep > 50% of *B* events.

- The data acquisition system saves all of the data in memory for as long as necessary to analyze each interaction (~ 1 millisecond on average for L1), and moves data to L2/3 processing units and archival data storage for selected interactions.
- The key ingredients that make it possible to meet this challenge:
  - BTeV pixel detector with its exceptional pattern recognition capabilities
  - Rapid development in technology – FPGAs, DSPs, microprocessors

FPGAs – field programmable gate arrays
DSPs – digital signal processors

Block Diagram of the Trigger & DAQ



Trigger Components WBS 1.8

- L1 pixel trigger (FPGAs, DSPs, L1 switch)
- L1 muon trigger (same hardware as L1 pixel trigger)
- Global Level 1 trigger (same DSP hardware)
- L2/3 hardware (Linux PC farm)
- L2/3 software (similar to HEP “offline” analysis)
- RTES software (fault detection and mitigation)

Base cost: $12.0M (Material: $6.9M, Labor: $5.1M)

+ $5M grant for RTES (NSF ITR program)

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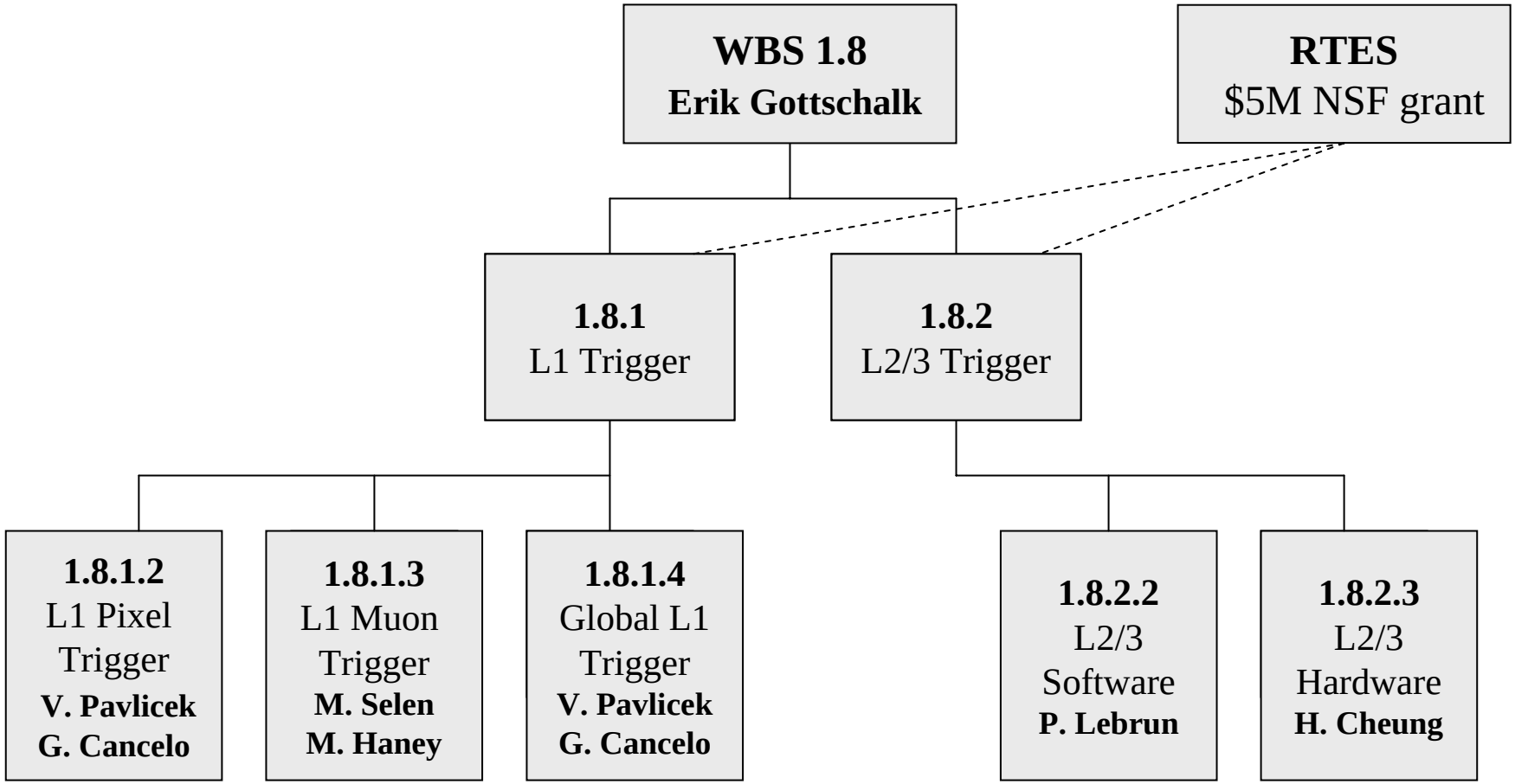

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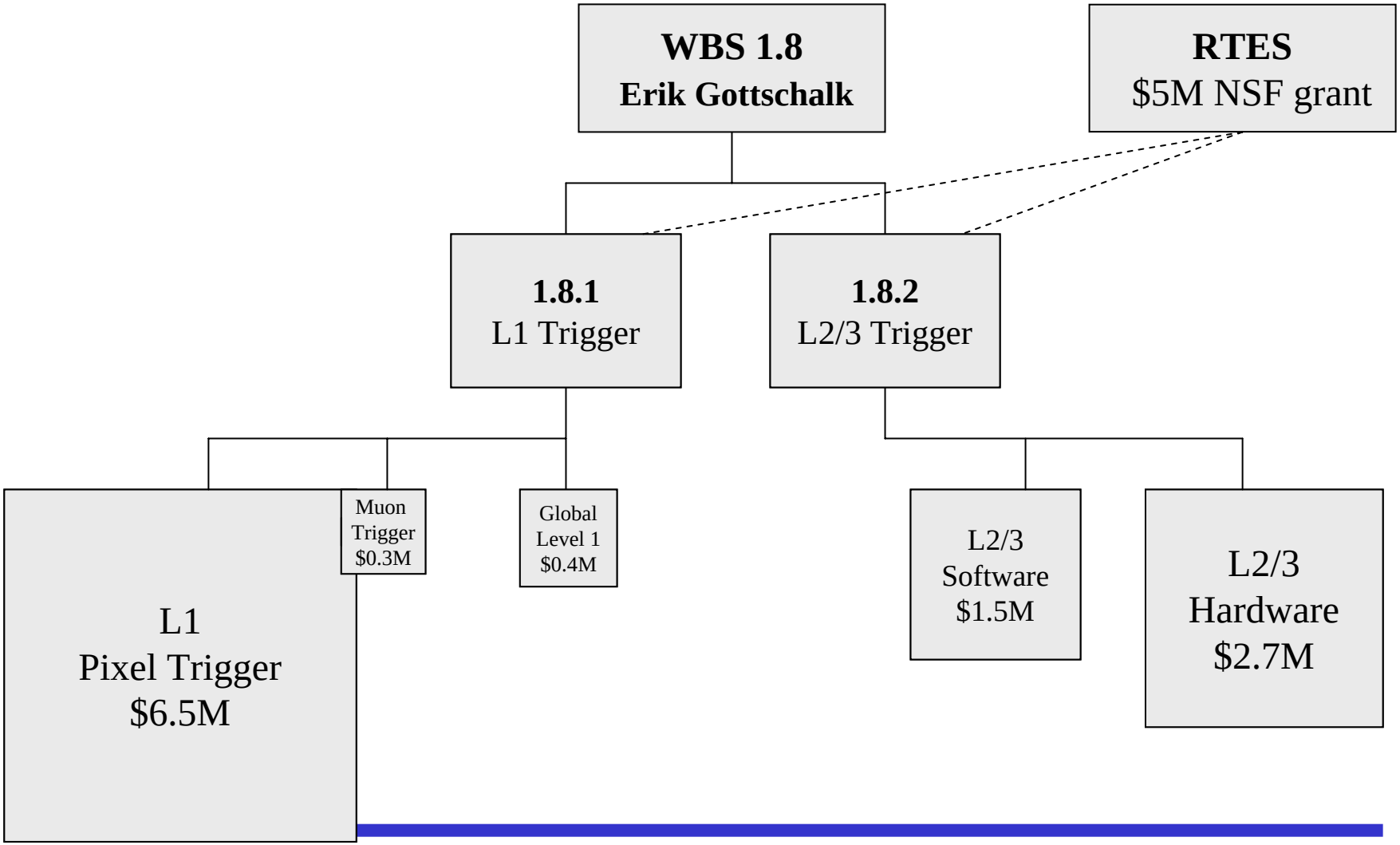
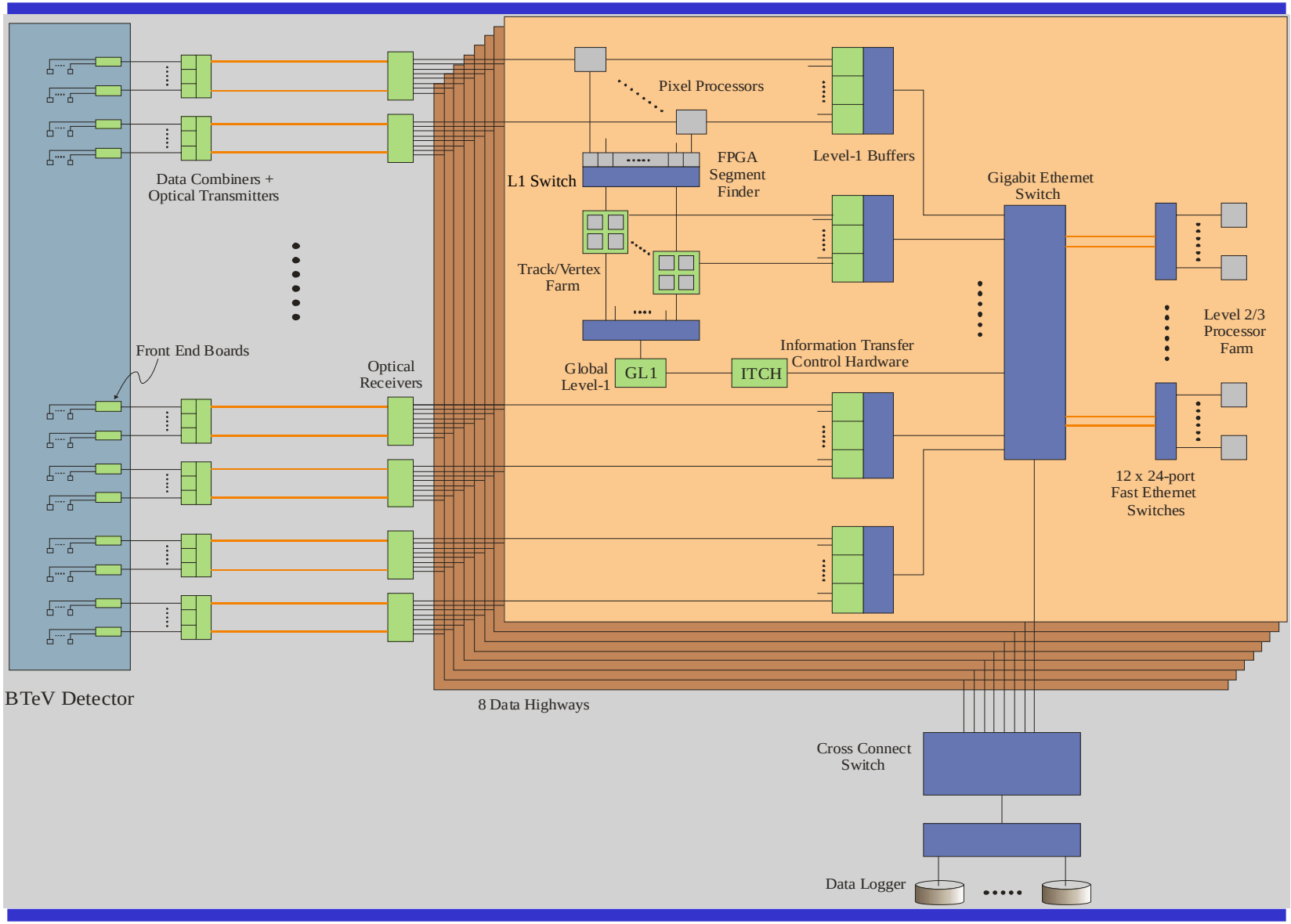
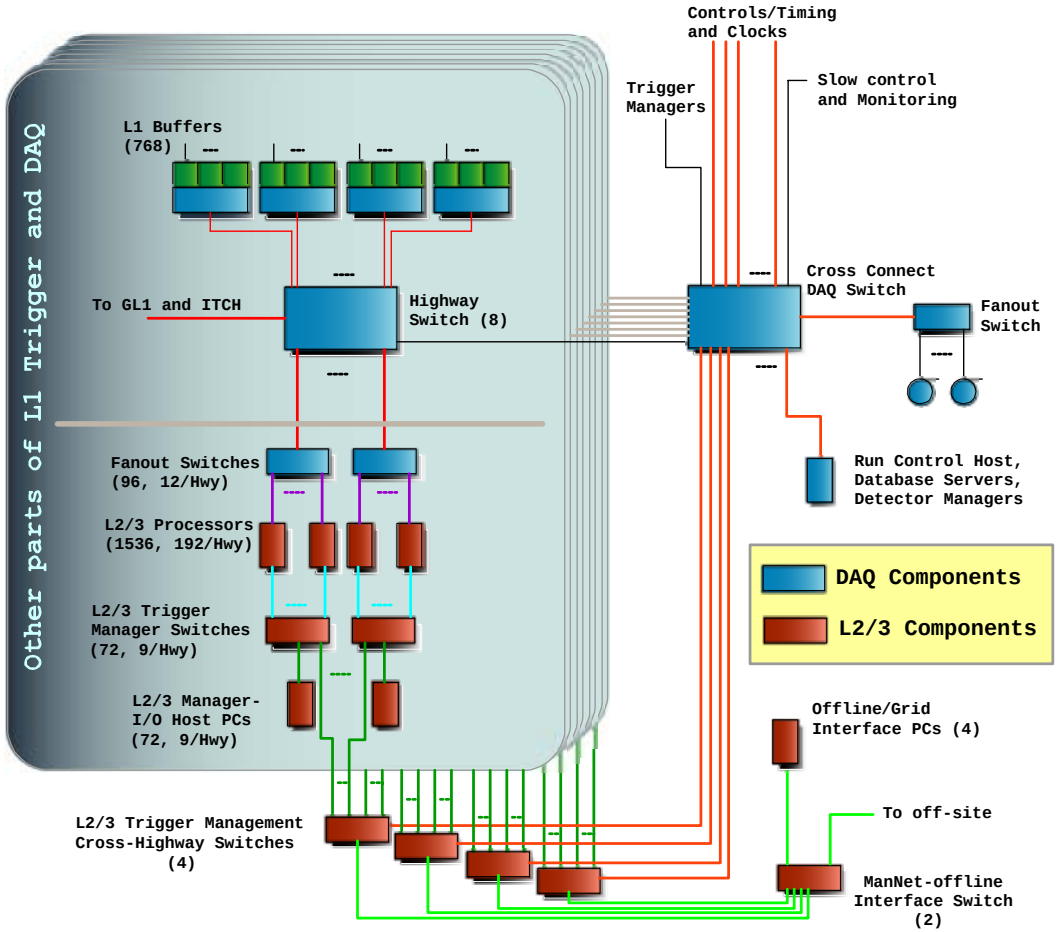


Three-level, eightfold trigger/DAQ architecture



L2/3 Trigger Hardware WBS 1.8



Baseline Design

- L2/3 Processor farm consists of 1536 “12 GHz” CPUs (dual-CPU 1U rack-mount PCs)
- L2/3 trigger includes Manager-I/O Host PCs for database caches, worker management, monitoring, and event pool cache
- L2/3 Hardware in 

L2 and L3 Trigger Software WBS 1.8

- L2 and L3 reconstruction software (tracks, photons, π^0's, Vees, particle ID, etc.)
- L2 and L3 trigger algorithms (selection criteria)
- Global L2 and Global L3 software (combinations of selection criteria and trigger lists)
- Alignment and Calibration software
- Monitoring and event display software
- Software framework utilities and interfaces to databases
- DAQ interface software (interfaces to actual DAQ hardware)
- Trigger specific system software (run control, control and monitoring, and databases)
- Offline filter and fast charm/beauty monitoring software (specific selection and monitoring software needed before full L2/3 operational)

Trigger R&D (1 of 2) WBS 1.8

- The FPGA segment-tracker algorithm (L1 pattern recognition) has been implemented on an Altera FPGA. This validates the algorithm, and provides a basis for cost estimates.
- Queuing simulations have been performed. Queue sizes and bandwidths are within reasonable margins.
- A 4-DSP prototype system has been built to validate the design of the L1 DSP farm, and to provide cost estimates for this part of the trigger.
- DSP timing studies have been performed for L1 pixel and L1 muon trigger algorithms on a Texas Instruments C6711 floating-point DSP. This provides a basis for cost estimates.
- A hash sorter has been developed to move DSP calculations to FPGAs, and an FPGA segment matcher is being investigated to move additional DSP calculations to FPGAs.

Trigger R&D (2 of 2) WBS 1.8

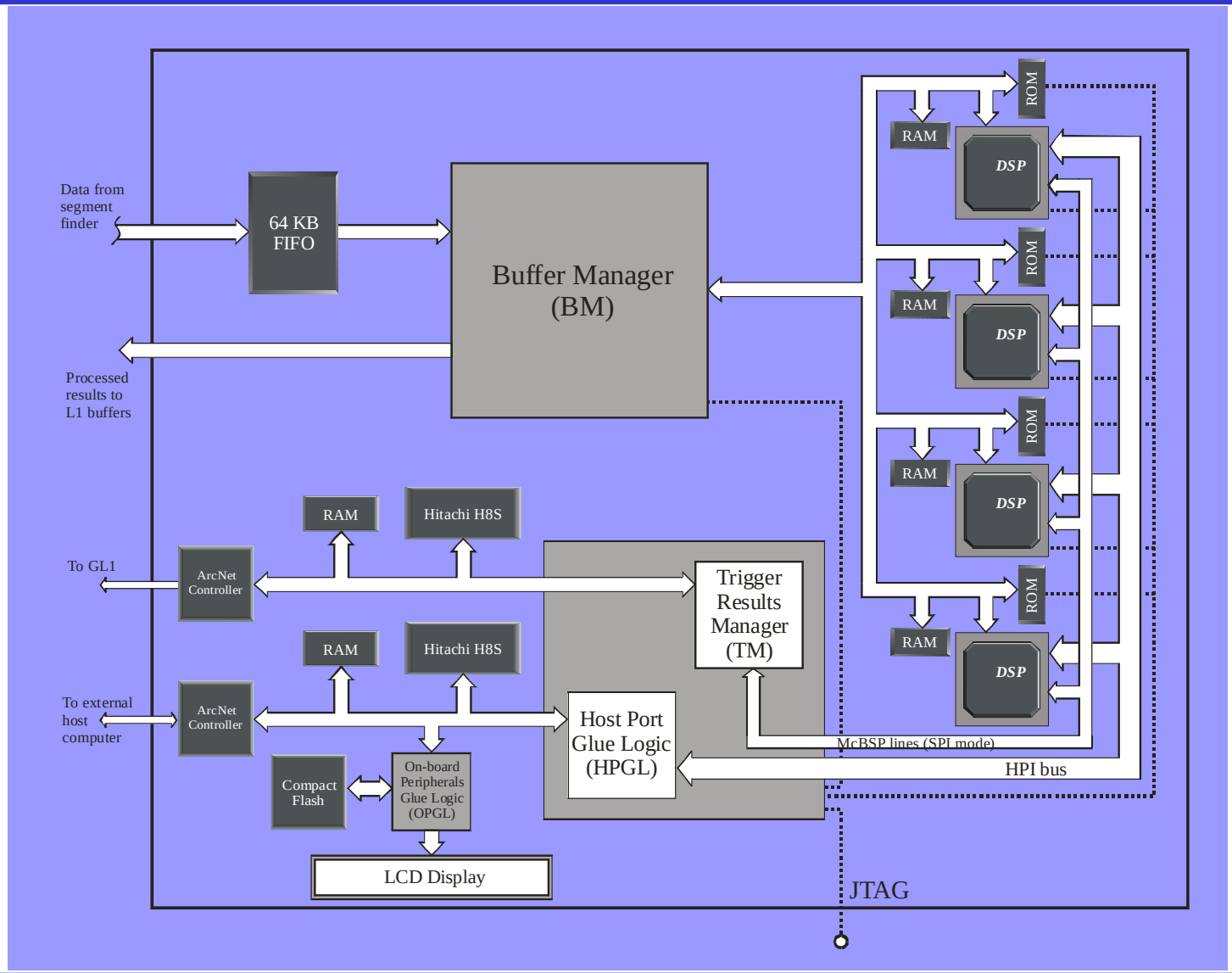
- Studies of alternative processors (e.g. Pentium and PowerPC processors) have been performed to see if there are other types of processors that could replace the DSPs in the L1 trigger. Results suggest that alternative processors exceed our performance estimates for the DSPs by factors of 2 to 3. These estimates are based on timing results for the L1 pixel trigger algorithm.

- An RTES demonstration system (hardware and software) has been developed and was presented at Super Computing 2003. The system consists of initial prototypes of RTES deliverables (GME models, ARMORs, and VLAs).

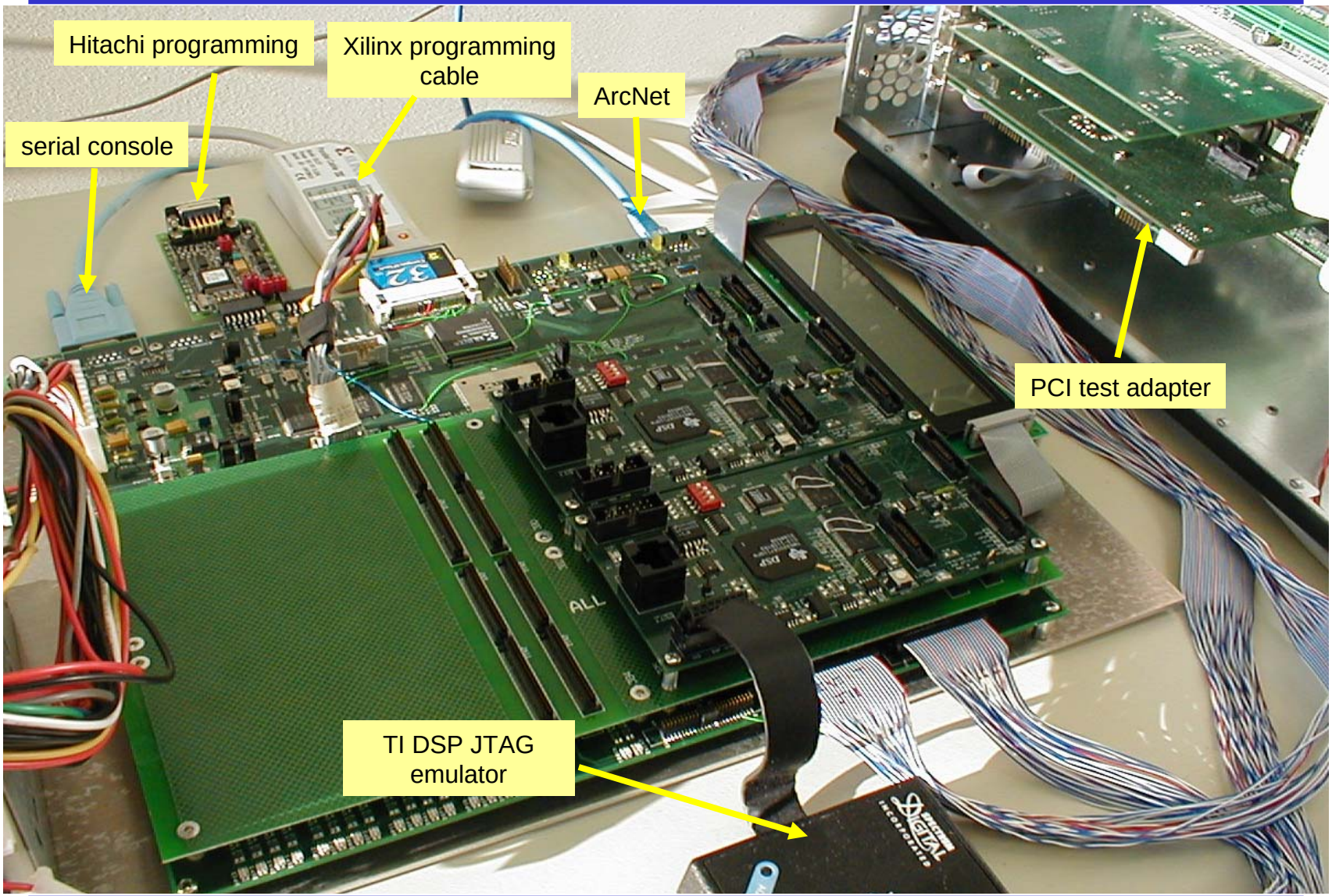
FPGA Segment Tracker R&D WBS 1.8

Modified version of PCI Test Adapter (PTA) card developed at Fermilab for testing hardware implementation of FPGA segment tracker

L1 DSP Farm R&D WBS 1.8



L1 Pre-prototype Test Stand WBS 1.8

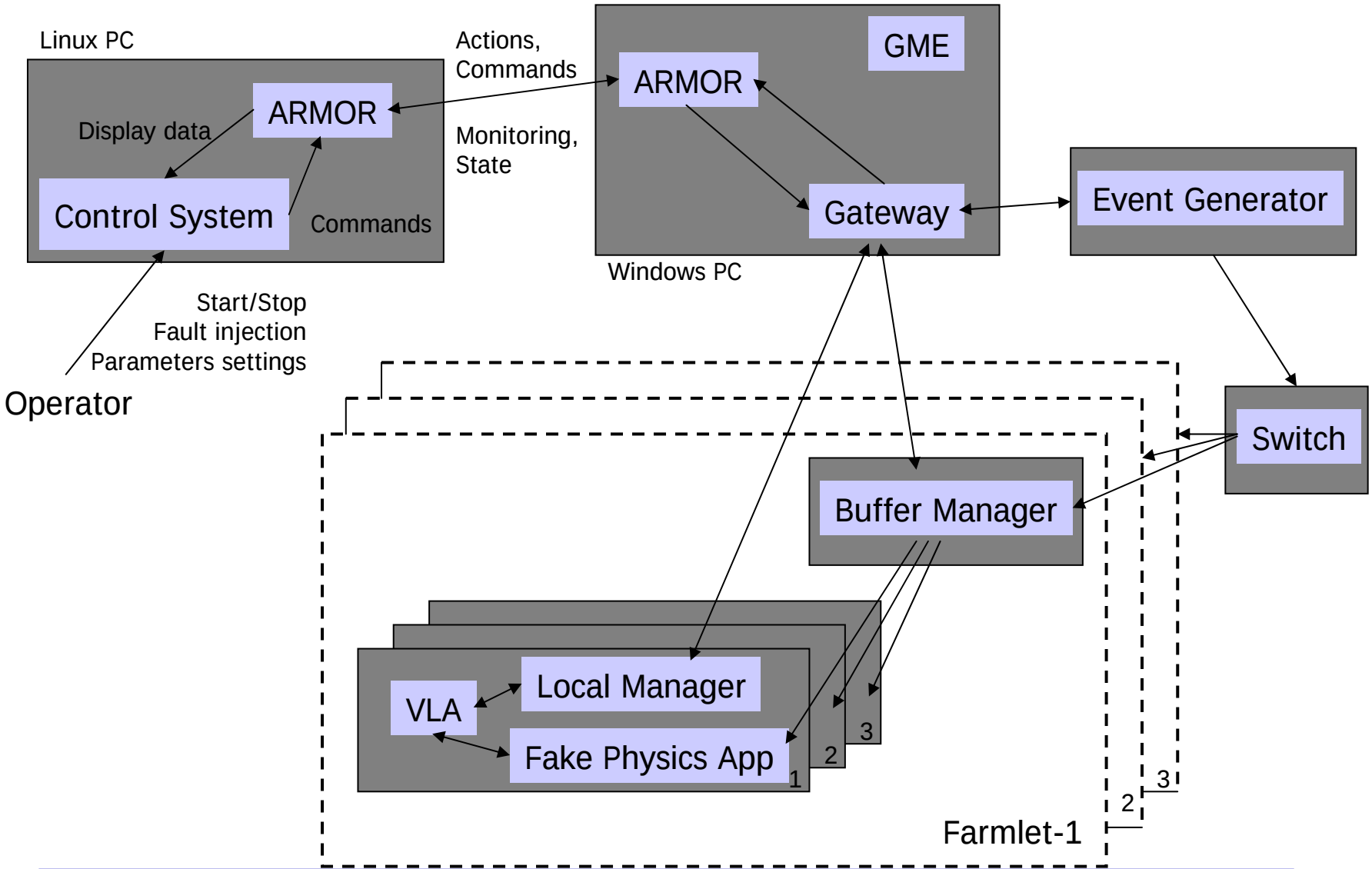


Size & Speed of L1 Muon Trigger Code WBS 1.8

- Work done at UIUC
  - Implemented “clock-cycle” counting technique for timing tests.
  - Optimized muon trigger code (used for simulations) for DSP
  - Achieved DSP results for efficiency & rejection that satisfy requirements
  - The results support the cost estimates for the L1 muon trigger

TMS320C6711

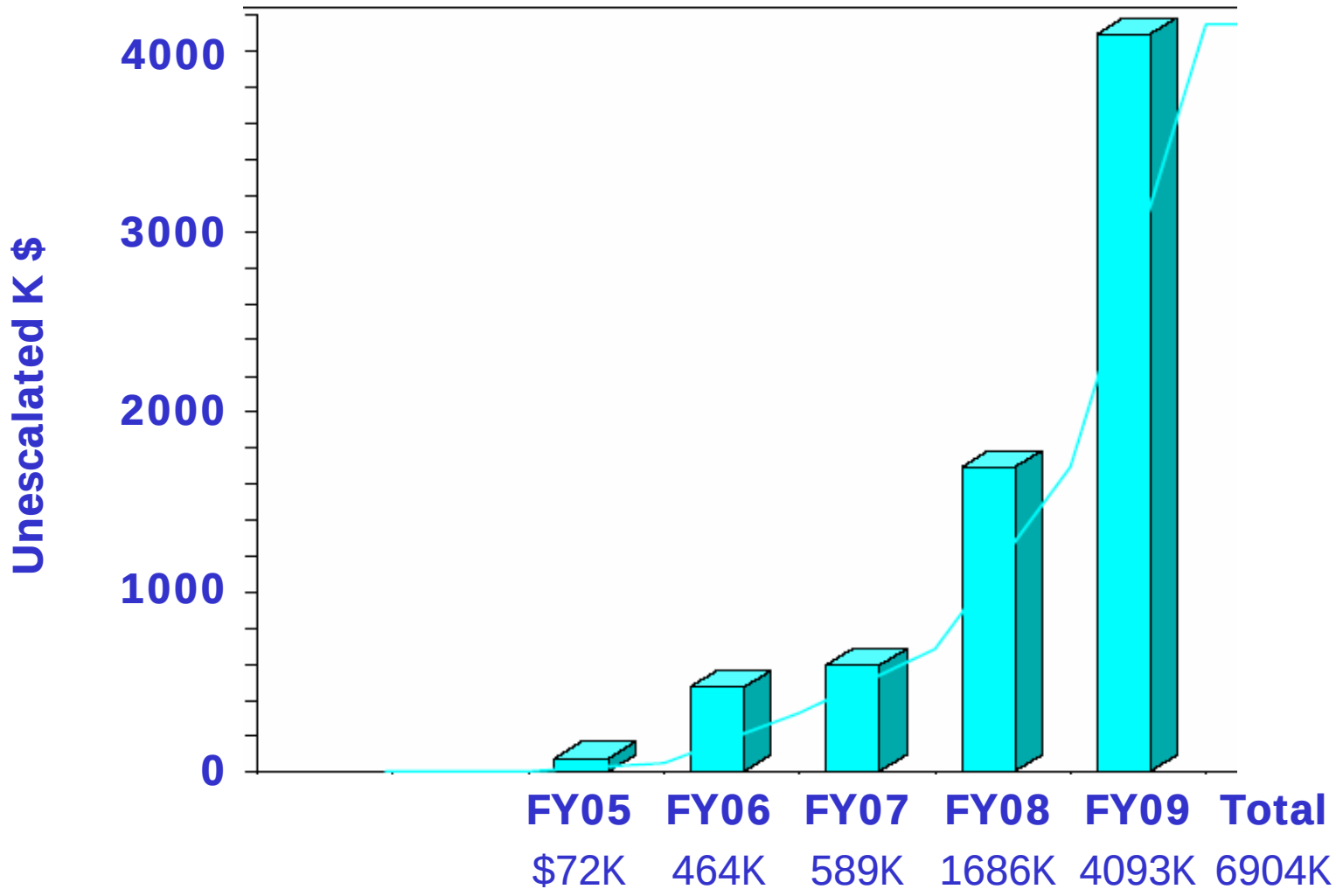
RTES Demo for Super Computing 2003 WBS 1.8



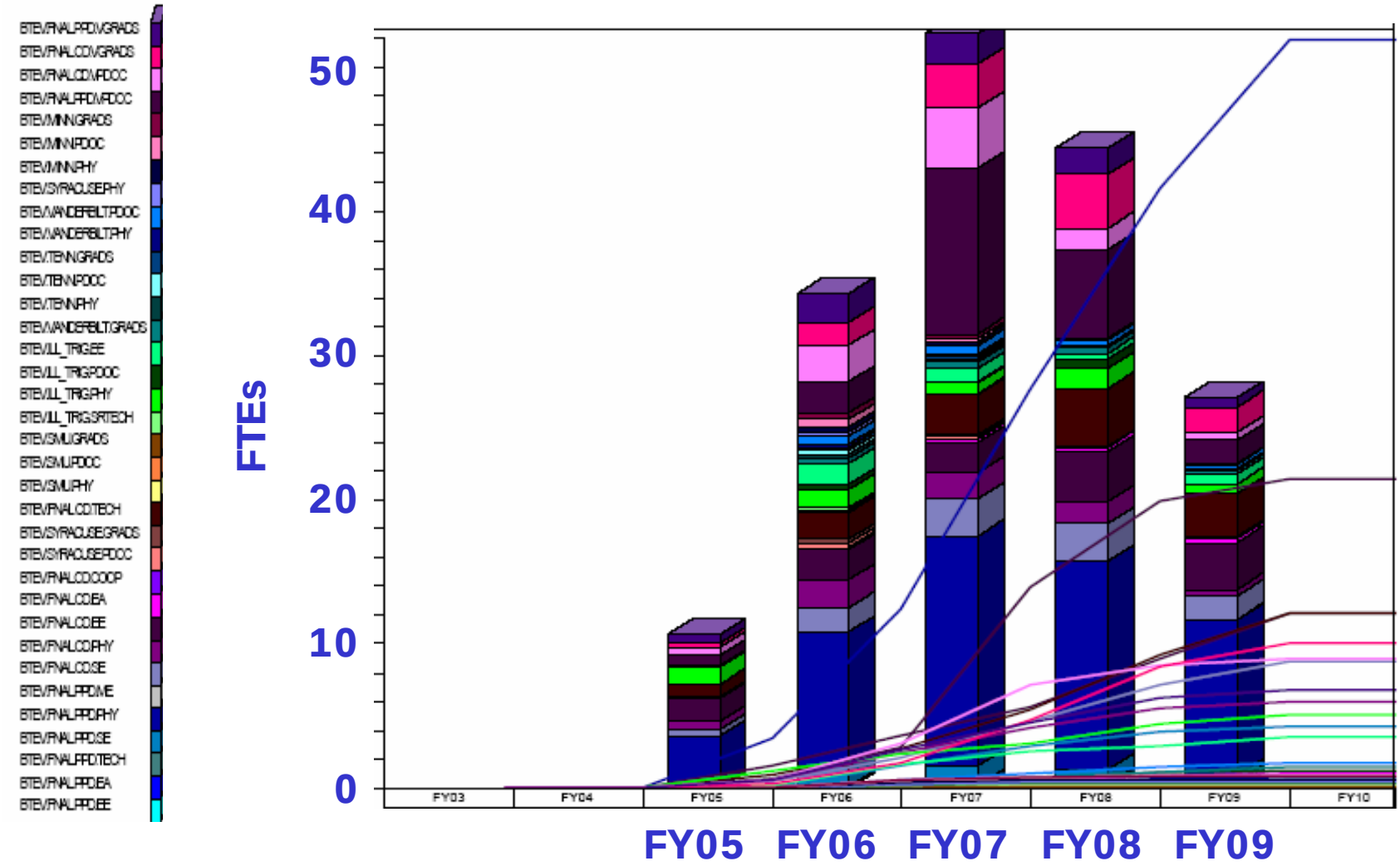
Construction Cost WBS 1.8

Activity ID	Activity Name	Base Cost ($)	Material Contingency (%)	Labor Contingency (%)	Total FY05	Total FY06	Total FY07	Total FY08	Total FY09	Total FY05-09
1.8.1	L1 Hardware & Software	7,432,834	32	33	471,742	1,177,055	1,484,092	2,846,048	3,867,232	9,846,170
1.8.2	L2/L3 Hardware & Software	4,215,468	34	89	66,026	871,834	1,067,147	1,559,965	3,141,053	6,706,025
1.8.3	Trigger Electronics & SW Subproj Mgmt	401,262	16	24	99,285	100,867	99,681	99,681	94,538	494,052
1.8	Subproject 1.8	12,049,564	33	53	637,053	2,149,757	2,650,919	4,505,693	7,102,824	17,046,246

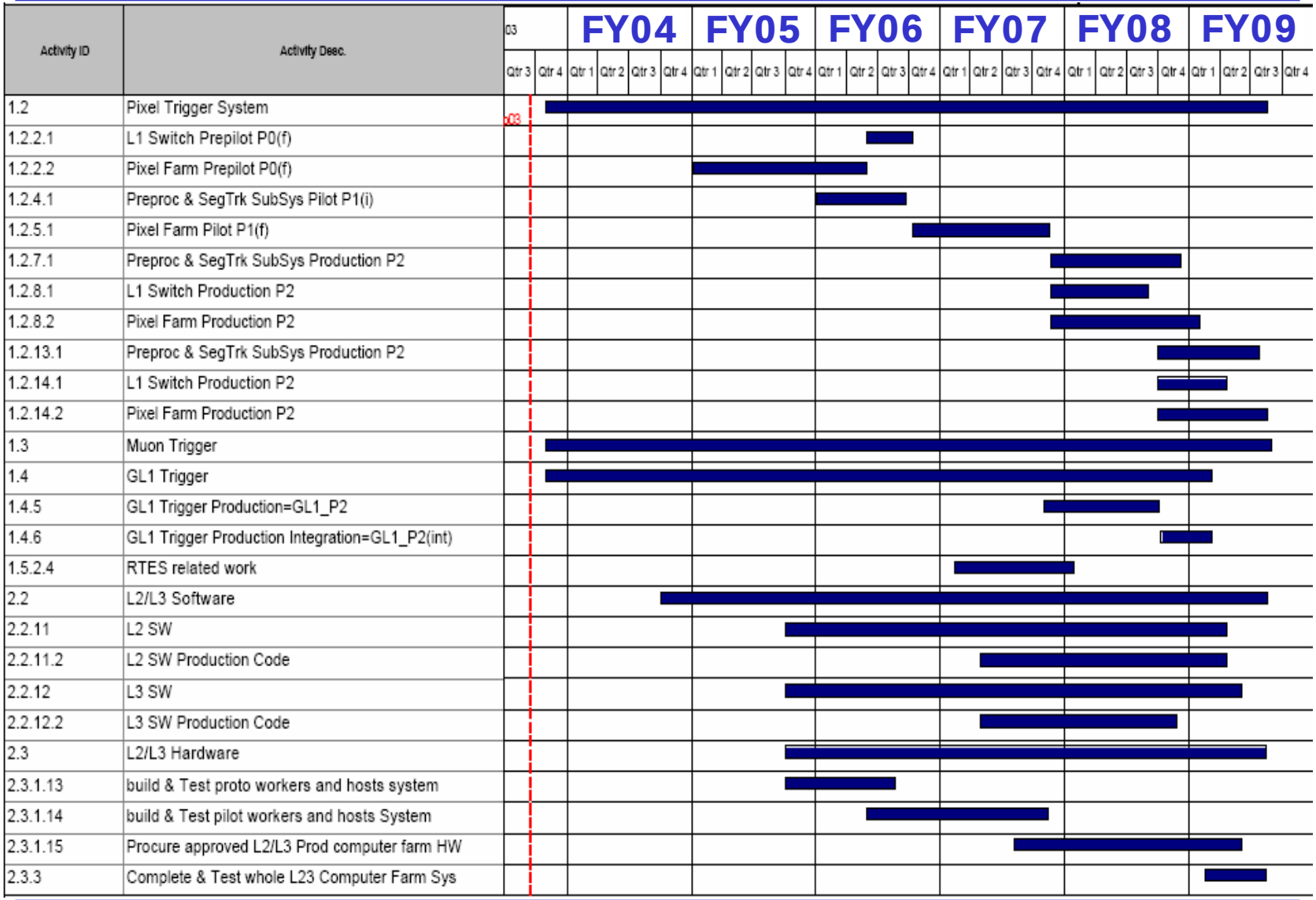
M&S Obligation Profile by Fiscal Year WBS 1.8



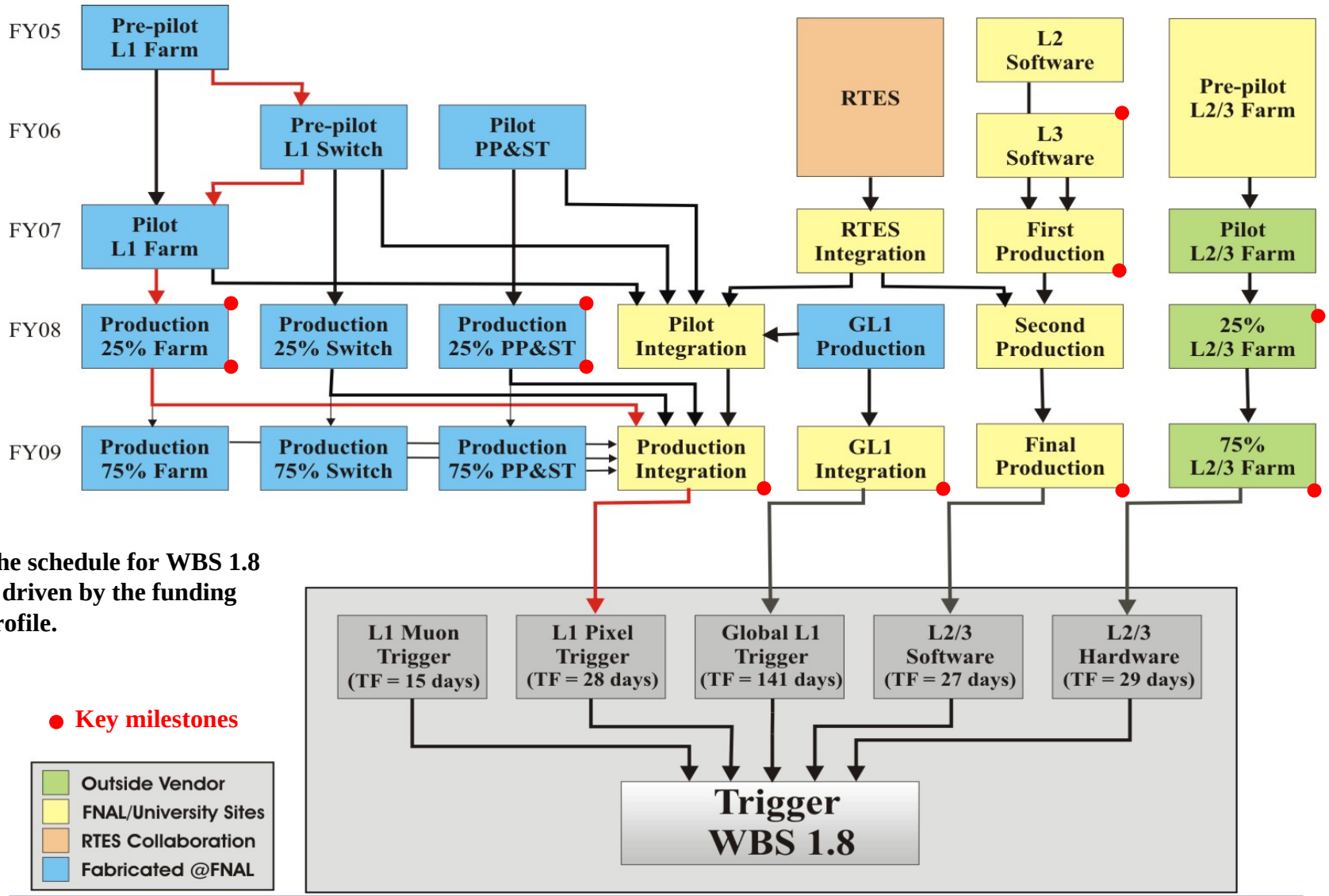
Labor Profile by Fiscal Year WBS 1.8



Gantt Chart WBS 1.8



Project Flow WBS 1.8



The schedule for WBS 1.8 is driven by the funding profile.

● **Key milestones**

Key Milestones WBS 1.8

L3	Begin L1 2-highway pixel processor & segment tracker production	Nov-07
L3	End L1 2-highway pixel processor & segment tracker production	Dec-08
L3	Begin L1 2-highway farm production	Nov-07
L3	End L1 2-highway farm production	Feb-09
L3	Begin L2/3 farm worker node procurement	Dec-07
L3	Begin L3 software development	Oct-05
L3	Complete first production release of L2/3 software	Jul-07
L3	Complete trigger system and integration with DAQ	Sep-09

Critical Path Analysis WBS 1.8

- L1 muon trigger (15 workdays of float)
  - Integration of the L1 muon trigger has the lowest total float in WBS 1.8. Integration activities begin in March, 2009 and are completed by September, 2009. The muon trigger integration depends on the fabrication of hardware developed for the L1 pixel trigger, and therefore it occurs late in the schedule.
  - There are several more near-critical paths related to muon trigger integration with TF = 17, 22, and 26.
- L1 pixel trigger (28 workdays of float)
  - The L1 pixel trigger has two production cycles (fabrication, assembly and testing) where 2 of the 8 highways (25% system) are built in FY08, and the remaining 6 highways (75% system) are built in FY09. The second production cycle has a total float of 28 days, begins in October 2008, and is completed in August 2009. Although we intend to have the entire trigger system operational by September 2009, BTeV is fully functional (with reduced capacity) with 2 of the 8 highways.

Critical Path Analysis WBS 1.8

- L2/3 software (27 workdays of float)
  - The L2/3 software that has the lowest total float is the fast charm and beauty monitoring software. The development of the software begins in March, 2009 and is completed in August, 2009. The development of the monitoring software is done late in the schedule, after the hardware and software infrastructure is in place.
- L2/3 hardware (29 workdays of float)
  - Like the production of the L1 pixel trigger, the production of the L2/3 hardware occurs in two production cycles with development of 2 highways (25% system) followed by the development of the remaining 6 highways (75% system). The first production cycle occurs in FY08, and the second in FY09.
  - The activity with the lowest total float is the completion and testing of the L2/3 hardware so that it is ready to be moved to C0. The start of this activity is delayed until the third of four shipments of farm worker nodes has arrived.

Risk Analysis WBS 1.8

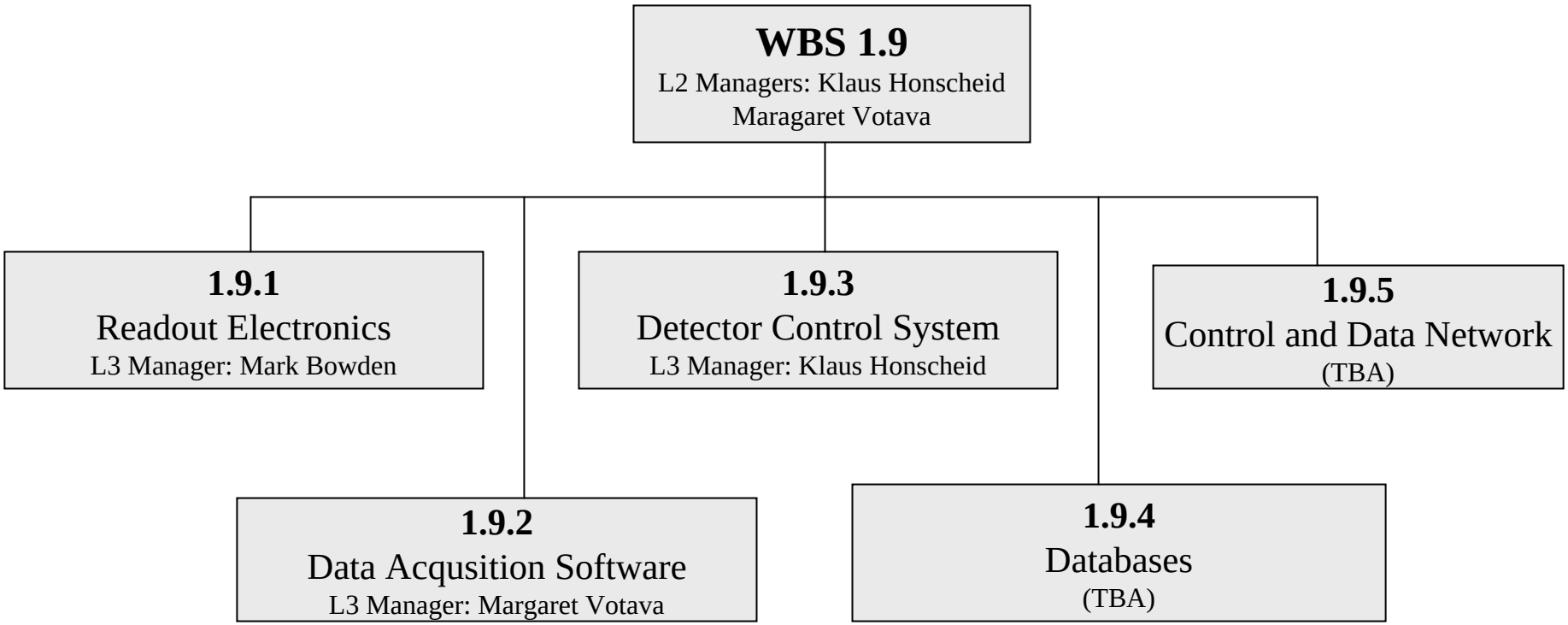
WBS Item	Risk Event	Response/Mitigation Strategy
For example: 1.8.1.2.2.2	Baseline processor fails to meet specified requirements	Benchmark and qualify more than one processor during R&D or early construction phase. Have 2nd option ready if 1st option is unsatisfactory.
For example: 1.8.1.2.4.1.2, 1.8.1.3.1.2	L1 pixel segment tracker or muon preprocessor algorithm exceeds the size of the selected FPGA. Larger FPGA increases the cost	Use contingency funds to upgrade to a bigger and more expensive FPGA. Consider other implementation alternatives early in the design stage. Consider simplifying the algorithms.
For example: 1.8.1.2.13.2	Communication links do not satisfy error rate specifications	Use contingency to fix PC boards, buy new parts, connectors, or cables.
For example: 1.8.1.2.8.2.3.3, 1.8.2.2.8	Shortage of software developers	Prioritize critical tasks. Use contingency to hire software developers temporarily.
Numerous WBS items	Experienced people leave	Be sure that more than one person is working on critical tasks. Use contingency funds to hire the person leaving as a temporary consultant while their expertise is transferred to existing or new personnel.

DAQ Components WBS 1.9

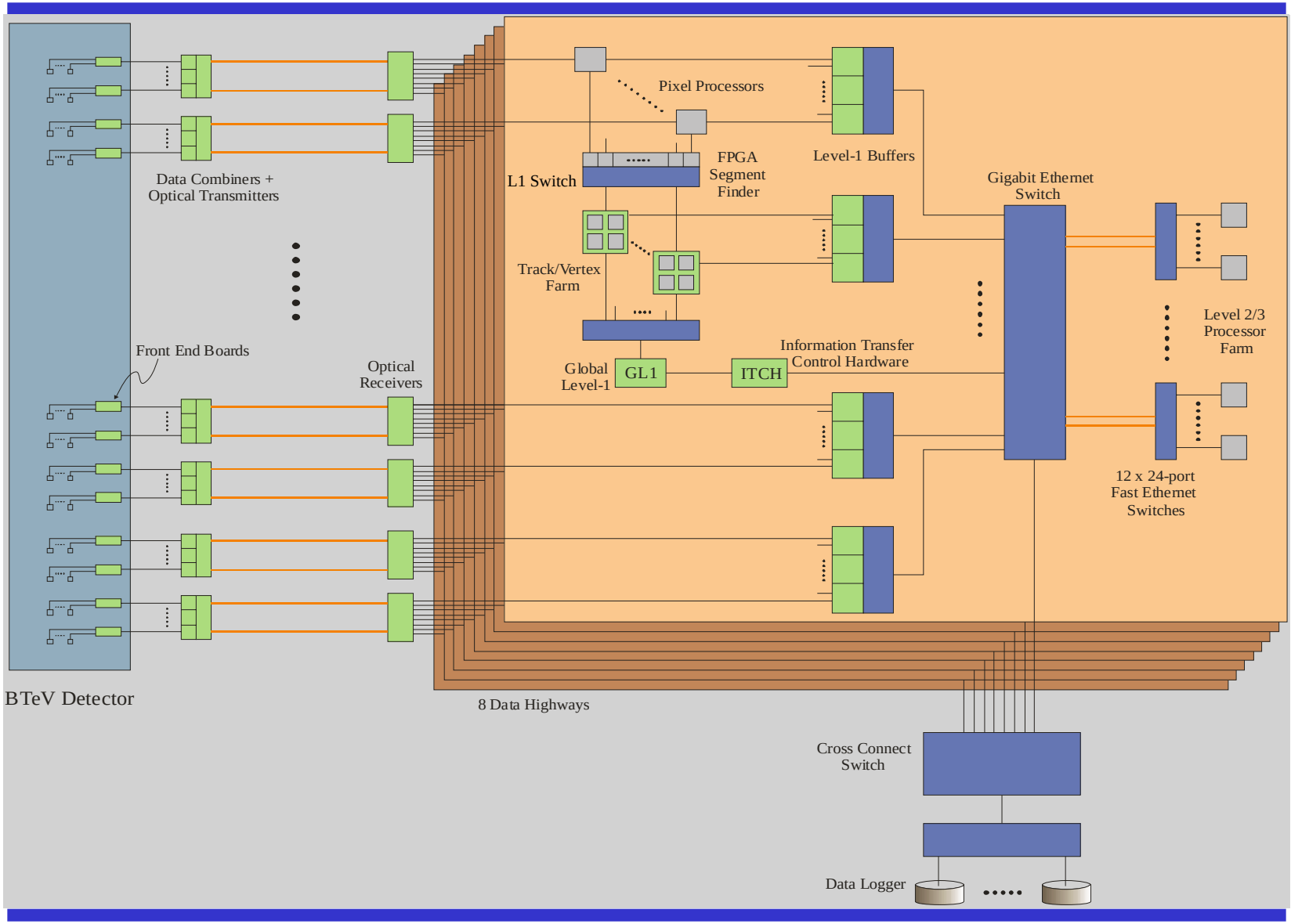
- Readout Electronics
- Data Acquisition Software
- Detector Control System
- Databases
- Control & Data Network

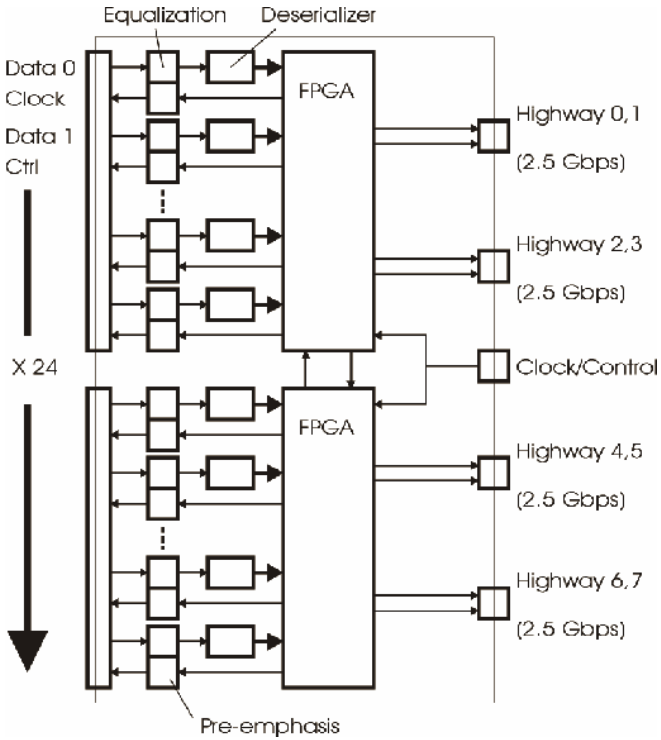
Base cost: $12.2M (Material: $5.2M, Labor: $7.0M)

Base cost: $12.1M (Material: $5.2M, Labor: $7.0M)

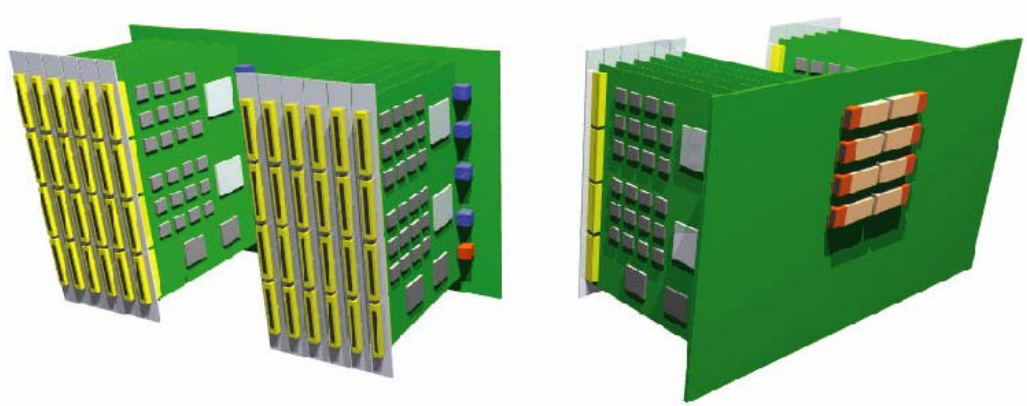


Three-level, eightfold trigger/DAQ architecture

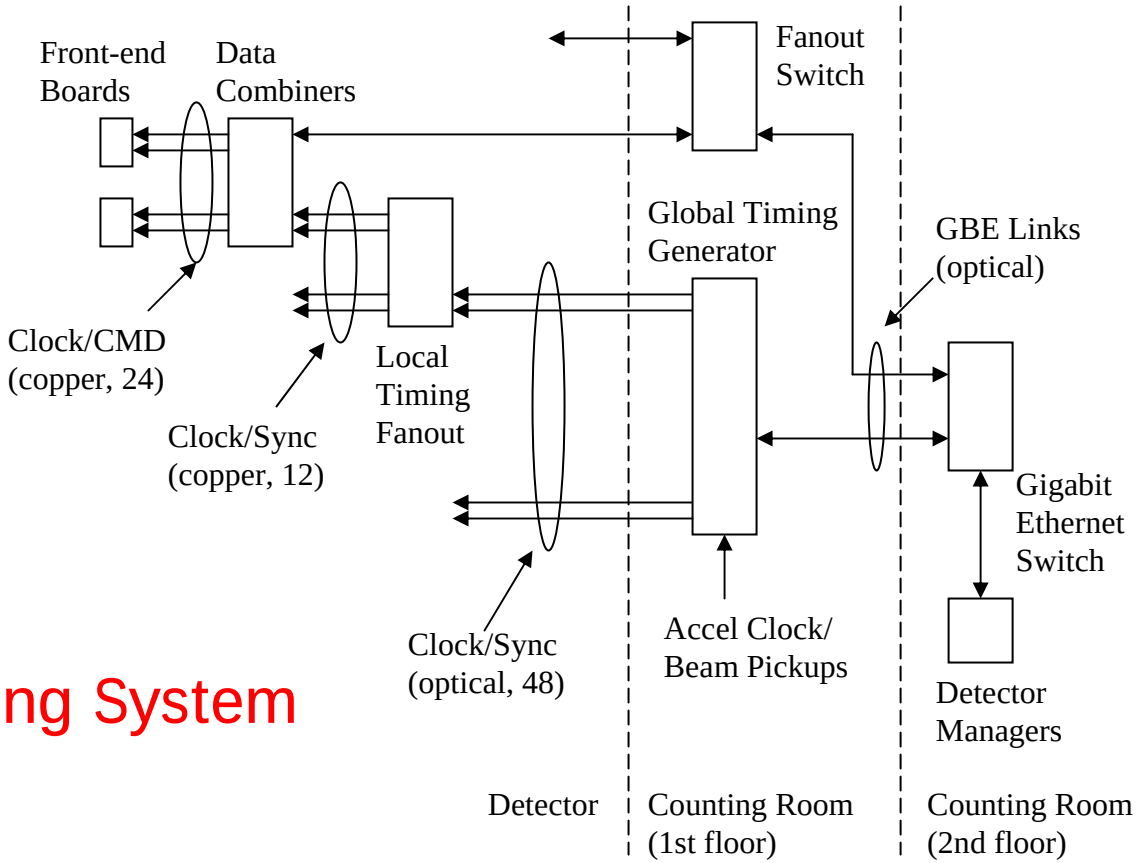




Data Combiner



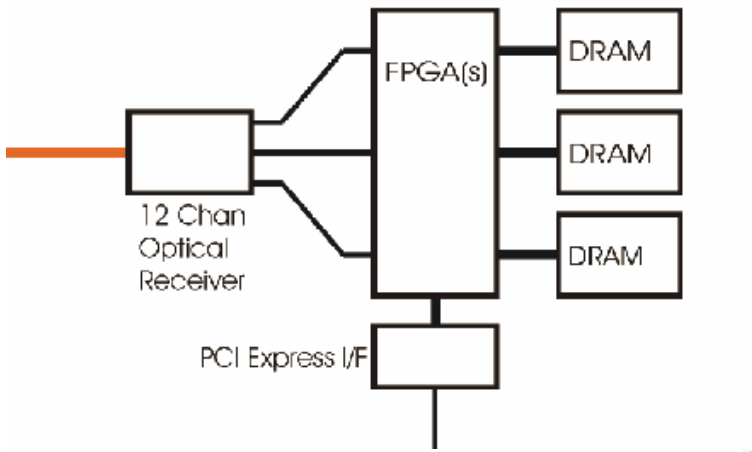
Input receiver/multiplexer for detector front-end boards.

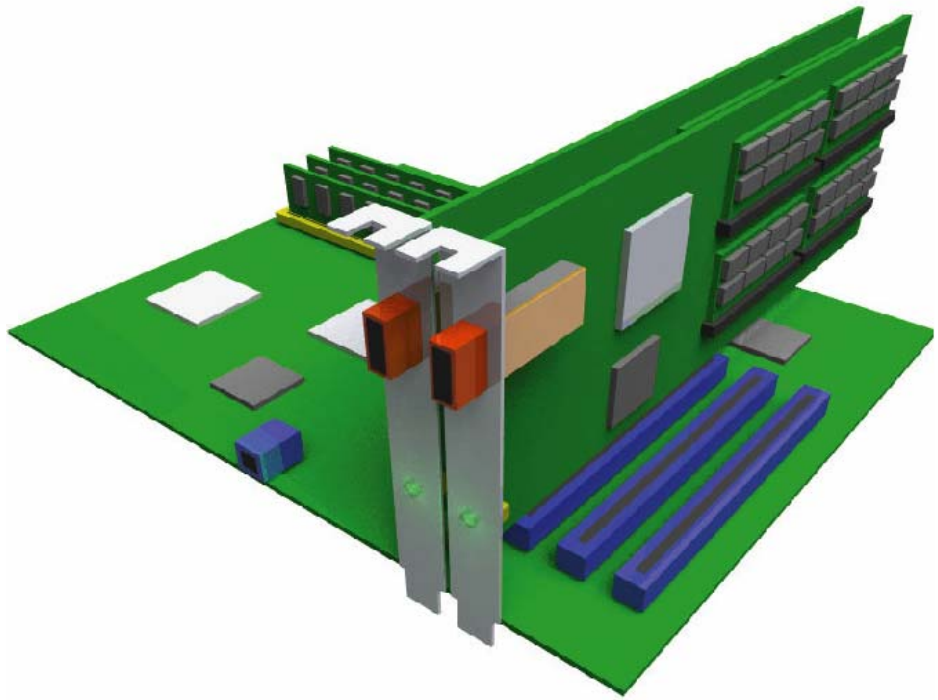


Timing System

Fast control and timing network for precise system synchronization.

Level 1 Buffer WBS 1.9



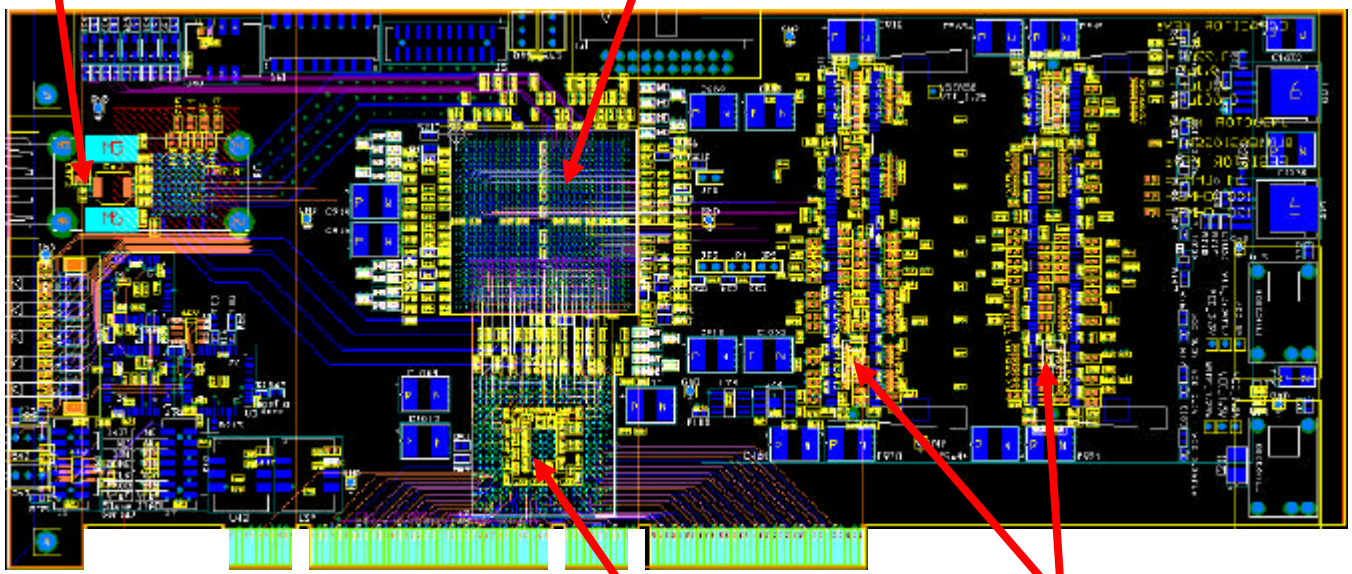


Large capacity buffers to hold detector data while L1 is processing pixel & muon data.

L1 Buffer Prototype WBS 1.9

Optical Receiver (12 channels X 2.5 Gbps)

FPGA (deserializers, memory controller)

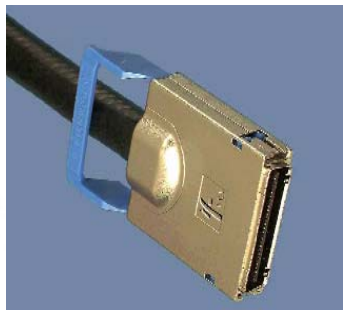


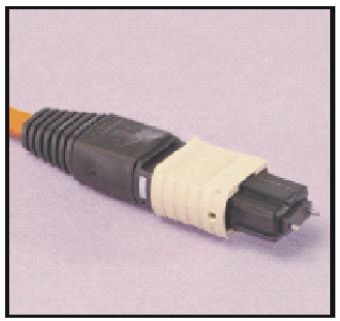
PCI Interface

DRAM (512 MB X 2, DDR SODIMM)

- Expect first boards in one month
- Standard optical interface
- Buffer memory architecture
- PCI Interface (BTeV will use a newer generation, maybe PCI-Express)

Data Links



Front-end to Data Combiners
- 600 Mbps copper

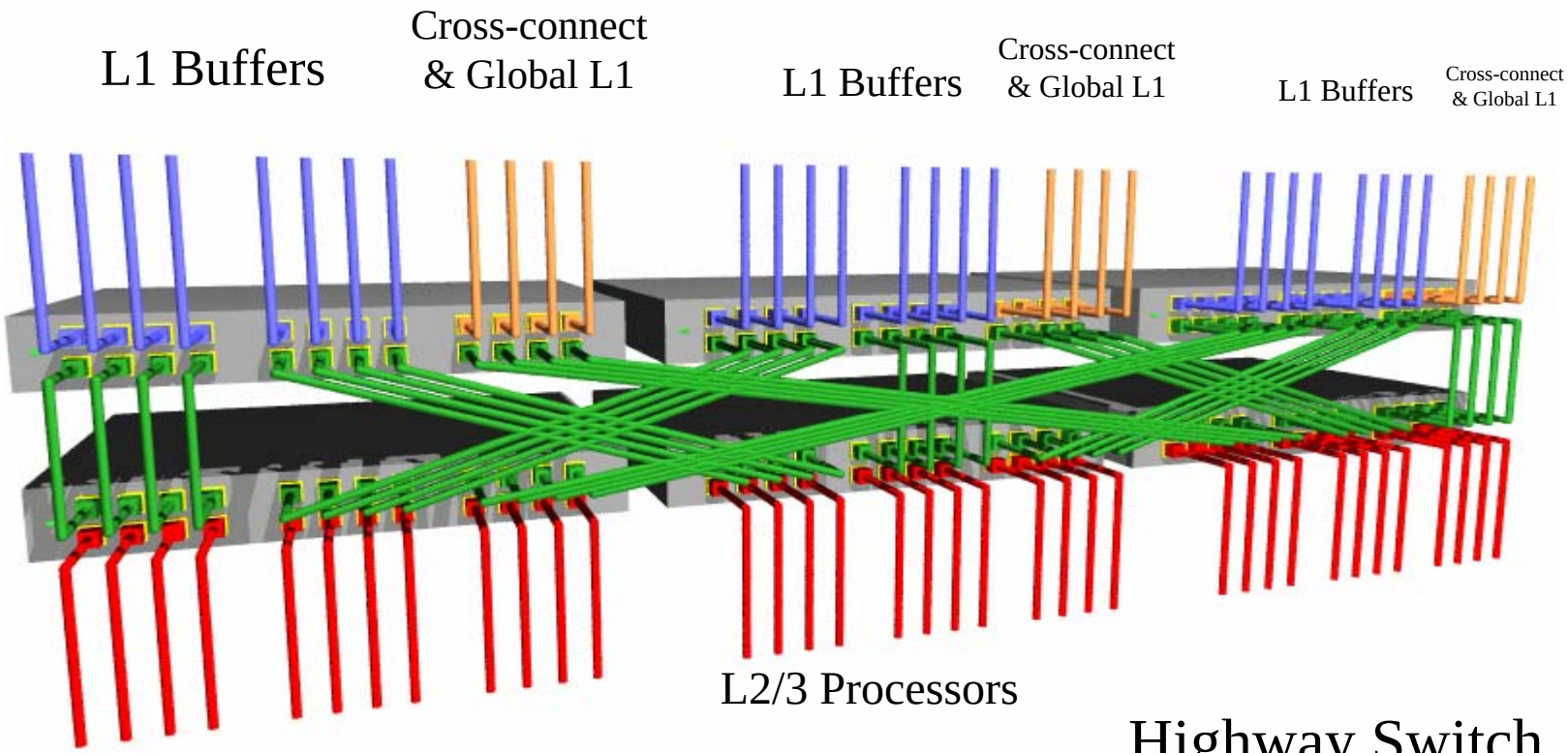
Data Combiners to L1 buffers & L1 Trigger
- 2.5 Gbps optical

L1 Trigger to L1 Buffers
- 2.5 Gbps copper

Network
- 1 Gbps (CAT6) copper

(all point-to-point serial)

Highway Switch (for a single highway) WBS 1.9



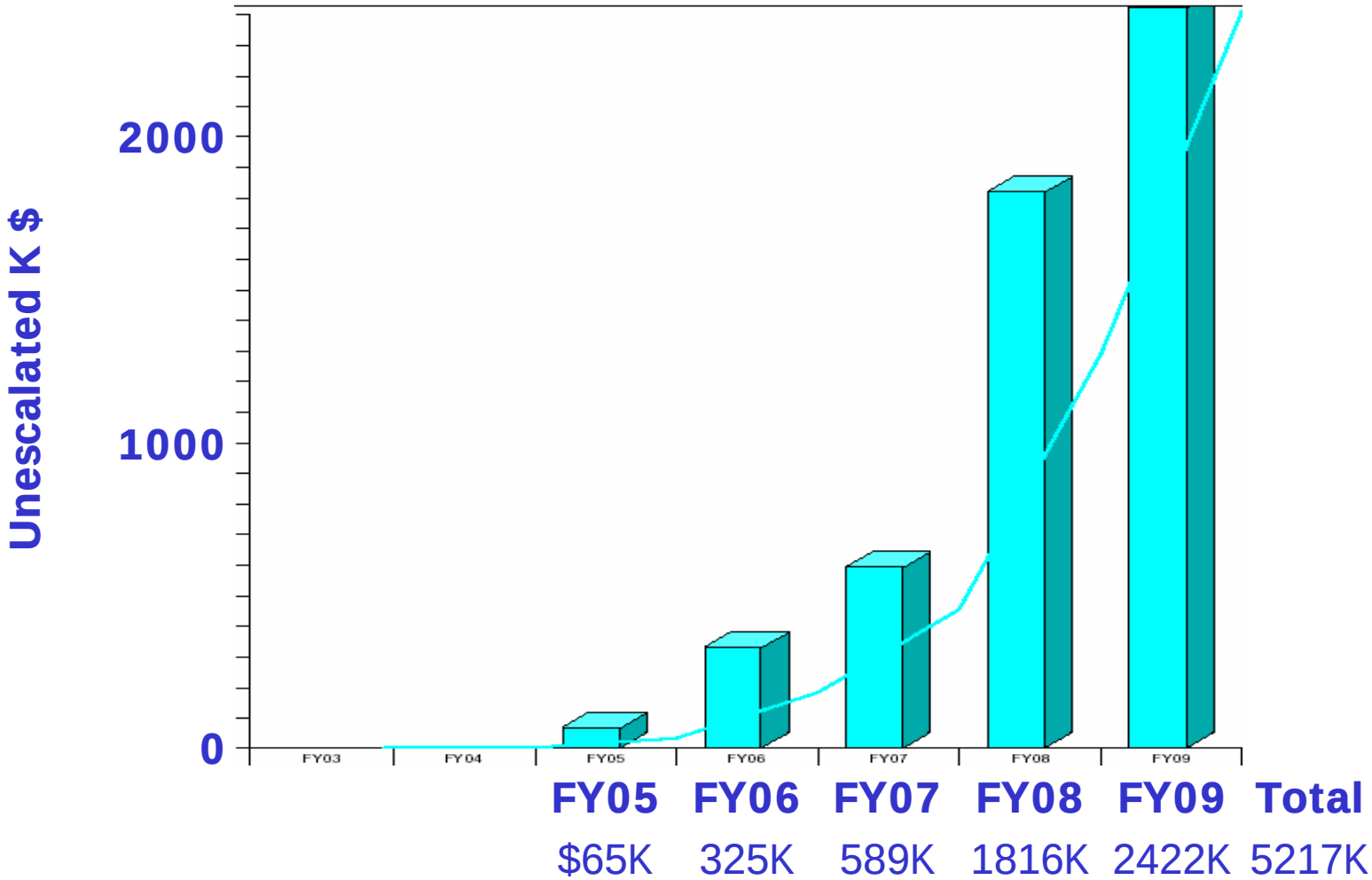
Other Major Components WBS 1.9

- Configuration Subsystem - software to download, initialize and partition all system components
- Run Control Subsystem - software to control and monitor the operation and overall dataflow of the system
- Detector Control - “slow” control network to set and monitor all system environmental parameters
- Databases - store and access operating parameters, maintain a time history of all system variables, and store and access parameters necessary for trigger algorithms
- Infrastructure - counting and control room infrastructure

Construction Cost WBS 1.9

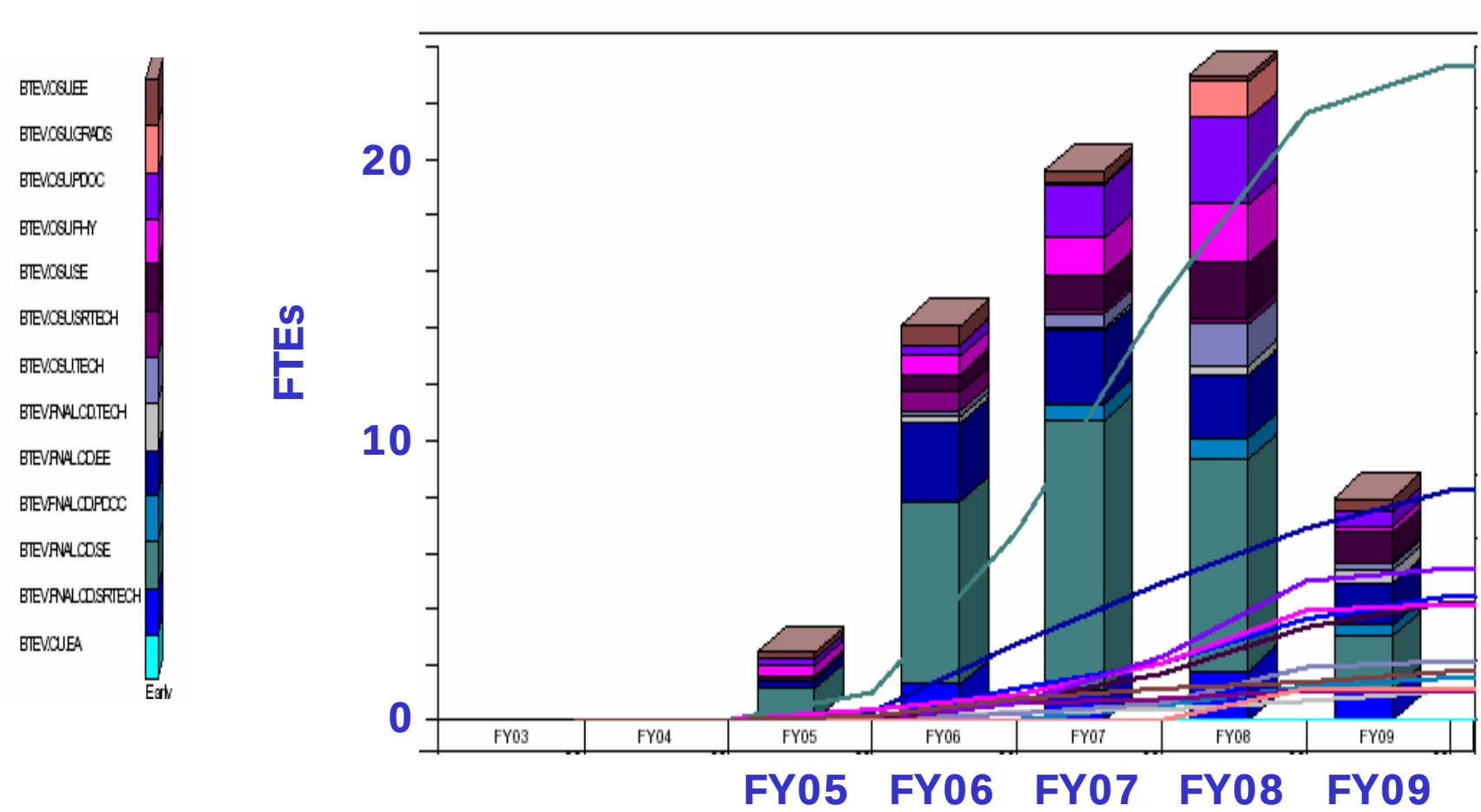
Activity ID	Activity Name	Base Cost ($)	Material Contingency (%)	Labor Contingency (%)	Total FY05	Total FY06	Total FY07	Total FY08	Total FY09	Total FY05-09
1.9.1	Readout Electronics	4,765,515	43	30	141,263	771,957	737,093	2,245,904	2,694,008	6,590,226
1.9.2	Data Acquisition Software	2,558,370	37	31	218,504	809,930	883,130	394,975	1,096,725	3,403,265
1.9.3	Detector Control System	520,613	26	30	0	0	266,307	324,009	74,649	664,965
1.9.4	Databases	1,478,585	60	29	0	539,804	640,968	677,859	100,581	1,959,212
1.9.5	Control & Data Network	392,923	60	30	0	0	283,967	0	271,655	555,622
1.9.6	Infrastructure & Integration	1,001,873	34	30	0	60,173	362,712	885,827	12,641	1,321,353
1.9.7	Technical Support Activities	1,426,606	34	25	22,962	476,790	386,878	550,934	358,027	1,795,590
1.9.8	Readout & Controls Subproject Management	36,192	30	0	10,269	10,433	10,310	10,310	5,728	47,050
1.9	**Subproject 1.9**	**12,180,678**	**41**	**29**	**392,998**	**2,669,086**	**3,571,366**	**5,089,817**	**4,614,014**	**16,337,282**

M&S Obligation Profile by Fiscal Year WBS 1.9



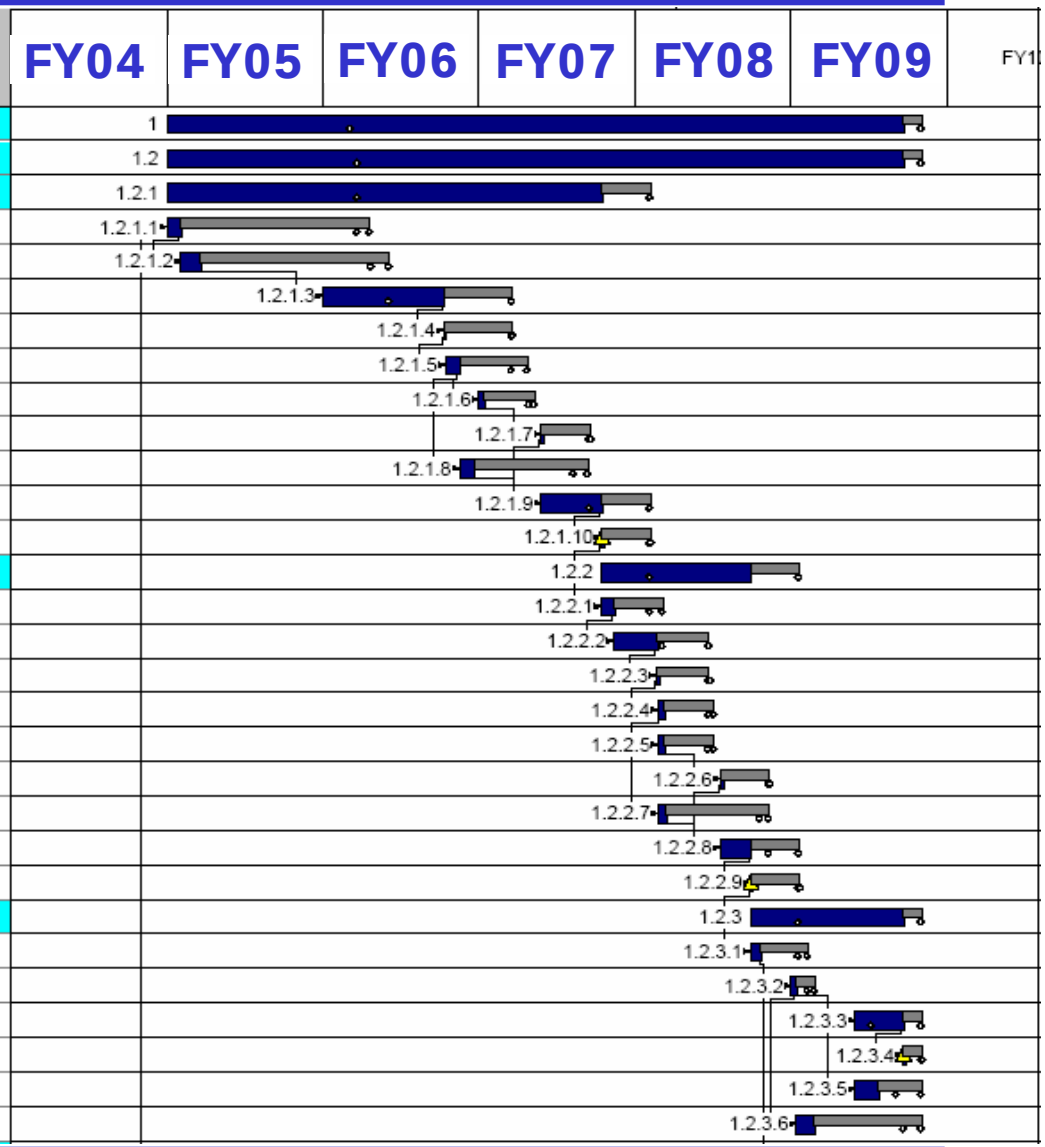
FY05	FY06	FY07	FY08	FY09	Total
$65K	325K	589K	1816K	2422K	5217K

Labor Profile by Fiscal Year WBS 1.9

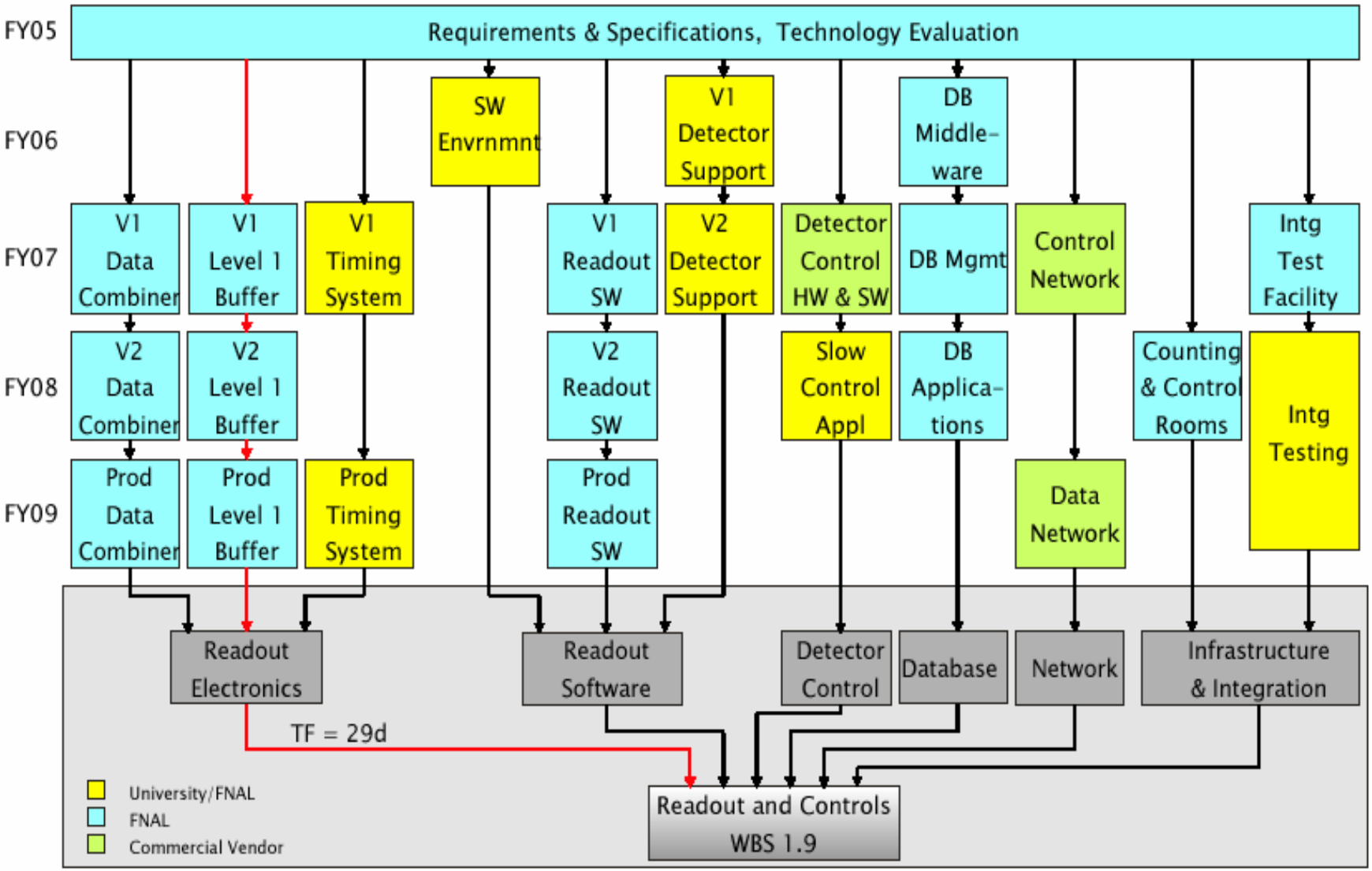


Gantt Chart WBS 1.9

Activity ID	Activity Description
1	Readout Electronics
1.2	Buffer SubSystem (L1B)
1.2.1	L1B-1 Design, Manufacture & Test
1.2.1.1	Lev3Rvw: Write & Review L1B Requirements Document
1.2.1.2	Lev3Rvw: Write & Review L1B Specifications Document
1.2.1.3	Lev3Rvw: Design & Review L1B Subsystem
1.2.1.4	Lev3Mil: L1B Design, Simulations and Layout Approved
1.2.1.5	Lev3Rvw: Write & Review L1B Manufacture, Assem and Test Spec
1.2.1.6	Order Manufacture, Assem and Test of First Version L1B
1.2.1.7	Lev3Mil: First Version L1B Delivered
1.2.1.8	Lev3Rvw: Write & Review L1B Test Procedures
1.2.1.9	Lev2Rvw: Test & Review First Version L1B
1.2.1.10	Lev2Mil: First Version L1B Test Results Approved
1.2.2	L1B-2 Design, Manufacture & Test
1.2.2.1	Lev3Rvw: Update & Review L1B Requirements & Specifications Doc
1.2.2.2	Lev3Rvw: Modify & Review Design and Layout of L1B Subsystem
1.2.2.3	Lev3Mil: L1B Design, Simulations and Layout Approved
1.2.2.4	Update L1B Manufacture, Assem and Test Spec
1.2.2.5	Order Manufacture, Assem and Test of Second Version L1B
1.2.2.6	Lev3Mil: Second Version L1B Delivered
1.2.2.7	Update L1B Test Procedures
1.2.2.8	Test Second Version L1B
1.2.2.9	Lev2Mil: Second Version L1B Test Complete
1.2.3	Production L1B Design, Manufacture & Test
1.2.3.1	Update Production L1B Manufacture, Assem and Test Spec
1.2.3.2	Order Manufacture, Assem and Test of Production L1Bs
1.2.3.3	Test Production L1Bs
1.2.3.4	Lev2Mil: Production L1Bs Delivered and Tested
1.2.3.5	Perform System Level L1B FMEA
1.2.3.6	Lev3Rvw: Write & Review L1B User's Guide and Operations Doc



Project Flow WBS 1.9



Key Milestones WBS 1.9

L2, L3	Data Combiner Board pre-production units tested and approved	Jul-07
L2	Multinode release of Data Acquisition RCS package	Aug-08
L3	Production DCB delivered and tested	Apr-09
L3	Production Level 1 Buffers delivered and tested	Jun-09
L3	Single node release of RCS package	May-07
L3	Data Acquisition software complete	Mar-09
L3	Calibration and Trigger database complete	Jul-08

Critical Path Analysis WBS 1.9

- Production L1 buffer (total float = 69 (29 + 40) workdays)
  - The production of the L1 buffer has the lowest float for WBS 1.9. The float results from several delays that are built into the schedule to match the funding profile for WBS 1.9.
- Data network installed (total float = 79 (39 + 40) workdays)
  - The installation of the complete data network will occur in FY09 to match the funding profile. A partial network will be completed in the second half of FY07 for use as a control network.
- Production DCB (total float = 108 (68 + 40) workdays)
  - The float for the production of the data combiner boards is determined by the funding profile for WBS 1.9.
- Data-logging hardware (total float = 129 (89 + 40) days)
  - The data-logging hardware is delayed until FY09 to take advantage of cost de-escalation for mass storage.

Note: 40 days of float have been added above to show the float relative to the end of construction in Sept. 2009 (the date that we used for WBS 1.9 in OpenPlan is August 1, 2009).

Risk Analysis WBS 1.9

WBS Item	Risk Event	Response/Mitigation Strategy
For example: 1.9.1.1	Data combiner boards are more sensitive to single-event upsets than expected	Implement redundant design in FPGA and plan for frequent downloads of firmware
1.9.4.1.2	Oracle license model changes to become exceedingly expensive	Switch to a freeware alternative, which is likely to increase the development time
For example: 1.9.1.4	Excessive bit-error rate on optical data links	Implement additional error correction (reduces overall bandwidth)
For example: 1.9.1.4	Detector data links do not operate at required rates	Replace data links with higher quality cables and/or connectors
Numerous WBS items	Lack of software development resources	Expand university participation

Summary for WBS 1.8 and WBS 1.9

More information on the trigger (WBS 1.8) and DAQ (WBS 1.9) is available in the breakout sessions.

WBS 1.8

- Overview – Erik Gottschalk
- L1 pixel trigger – Gustavo Cancelo
- L1 muon trigger – Mike Haney
- Global L1 trigger – Vince Pavilicek
- L2/3 software – Paul Lebrun
- L2/3 hardware – Harry Cheung
- RTES – Jim Kowalkowski

WBS 1.9

- Overview – Klaus Honscheid
- Readout and controls hardware – Mark Bowden
- Readout and controls software – Margaret Votava